

Title: ZERO DRIFT ANALOG MEMORY CELL,
ARRAY AND METHOD OF OPERATION

Applicant: George E. Gerpheide

Application No.: 10/822,555

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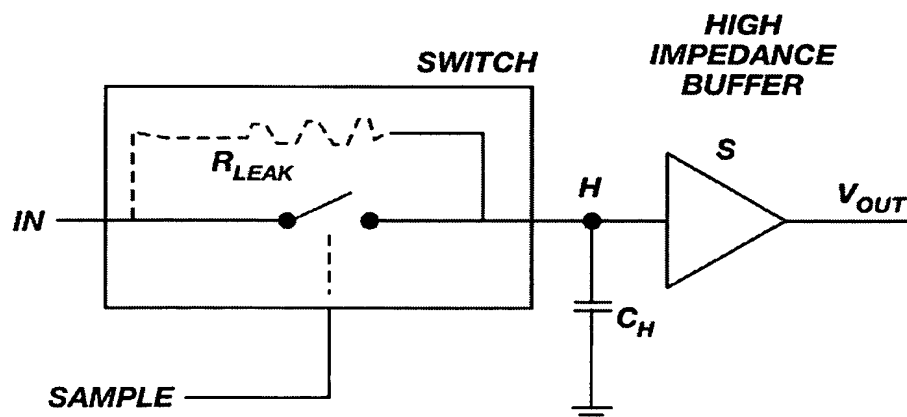


FIG. 1
(PRIOR ART)

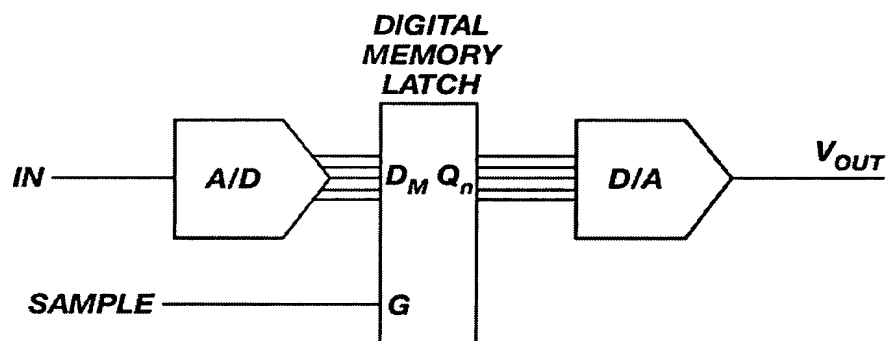


FIG. 2
(PRIOR ART)

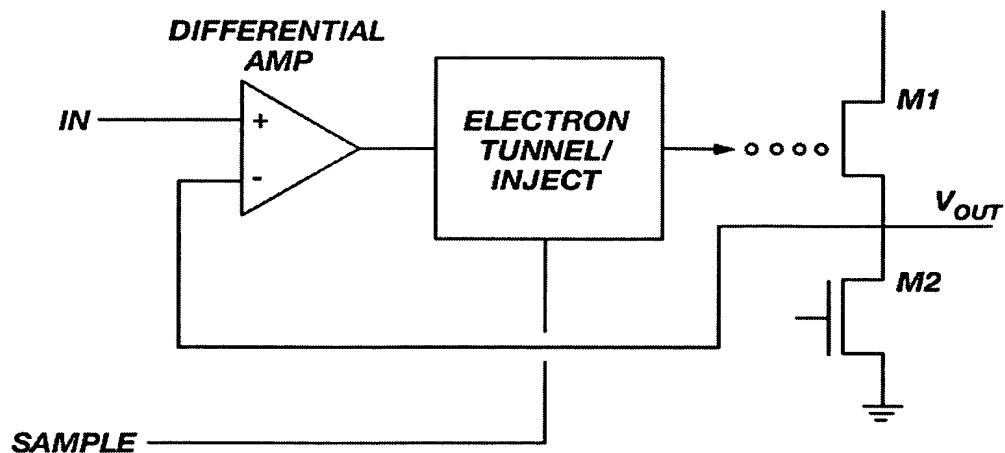


FIG. 3
(PRIOR ART)

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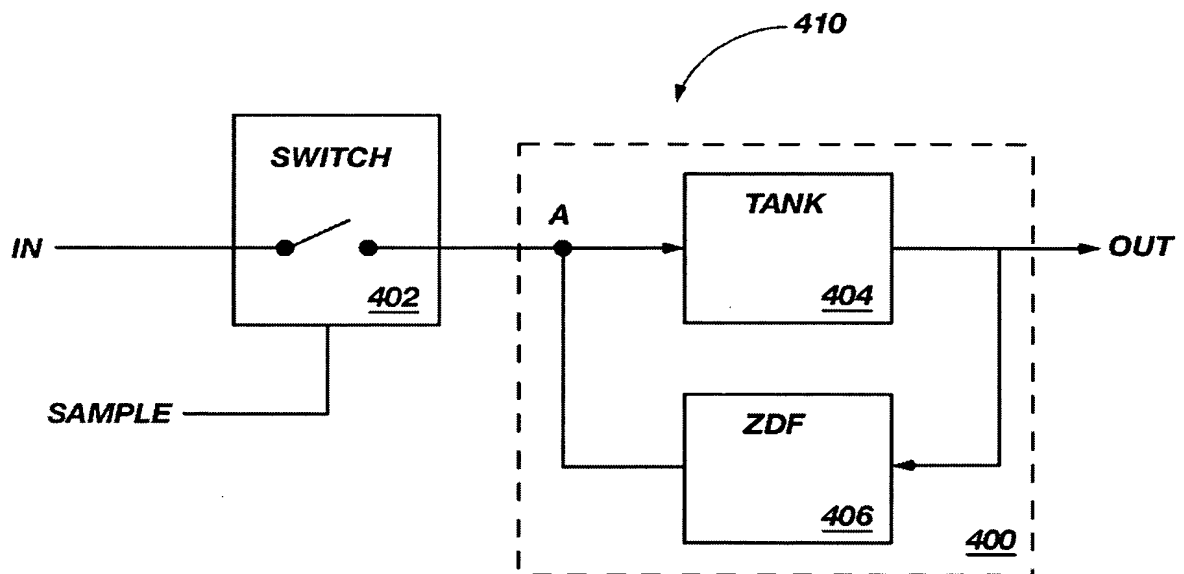


FIG. 4

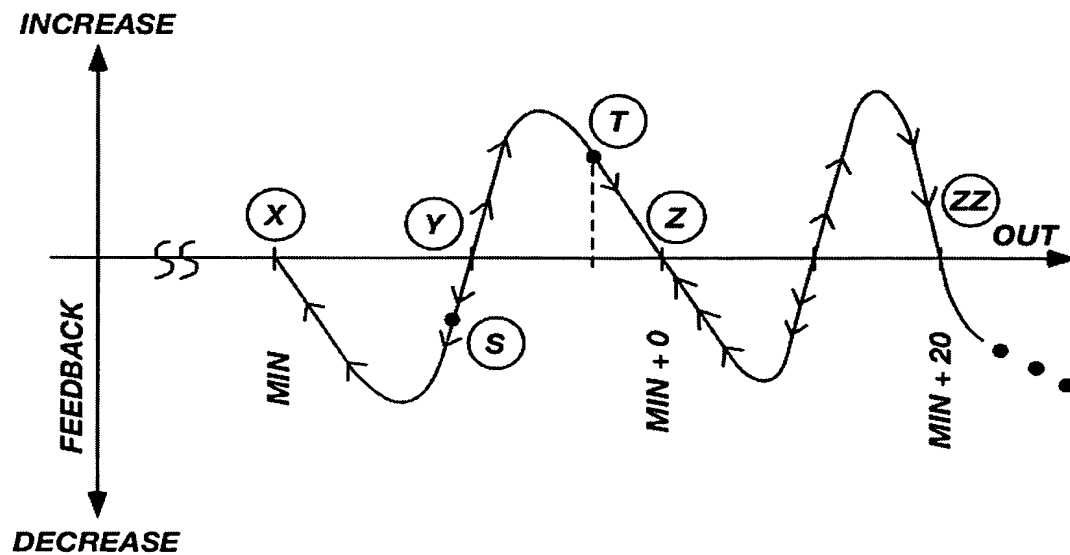


FIG. 5

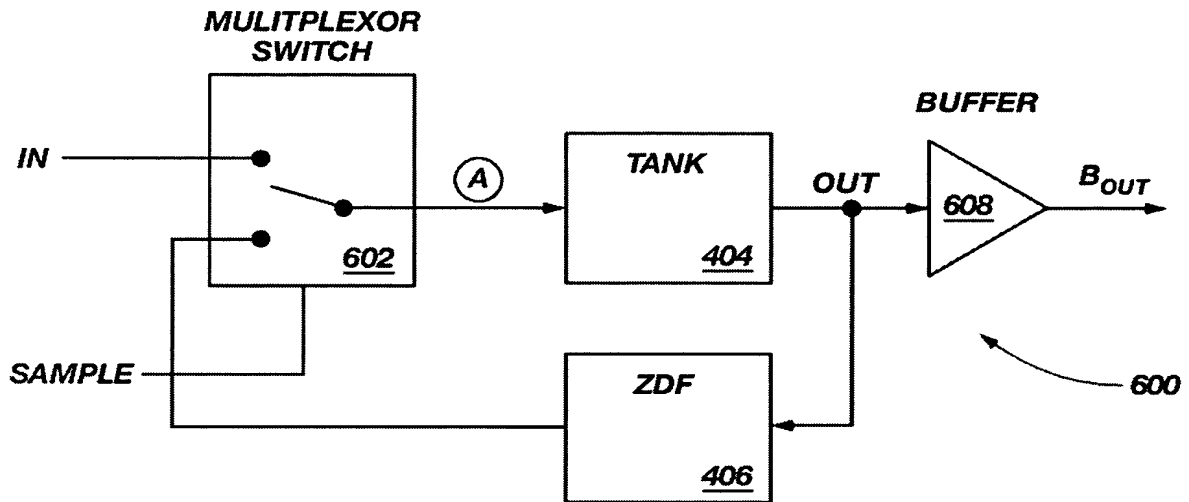


FIG. 6

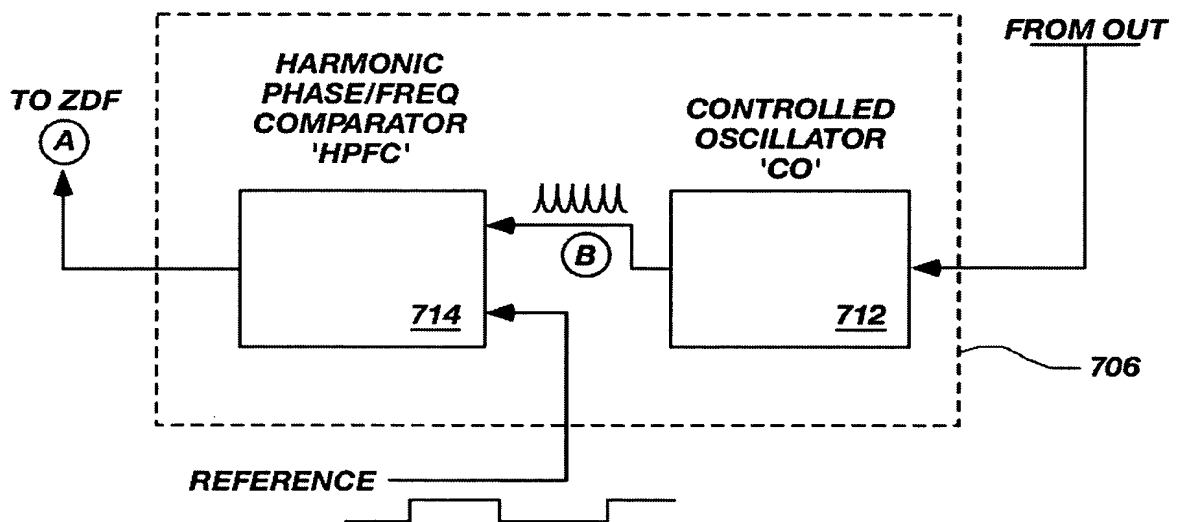


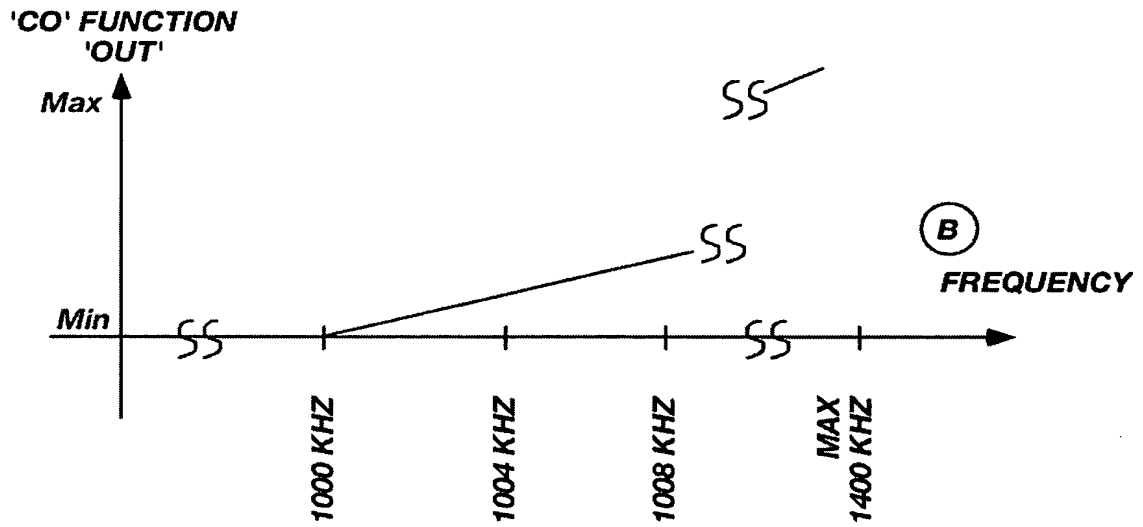
FIG. 7

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DECREASE

'HPFC' FUNCTION
INCREASE

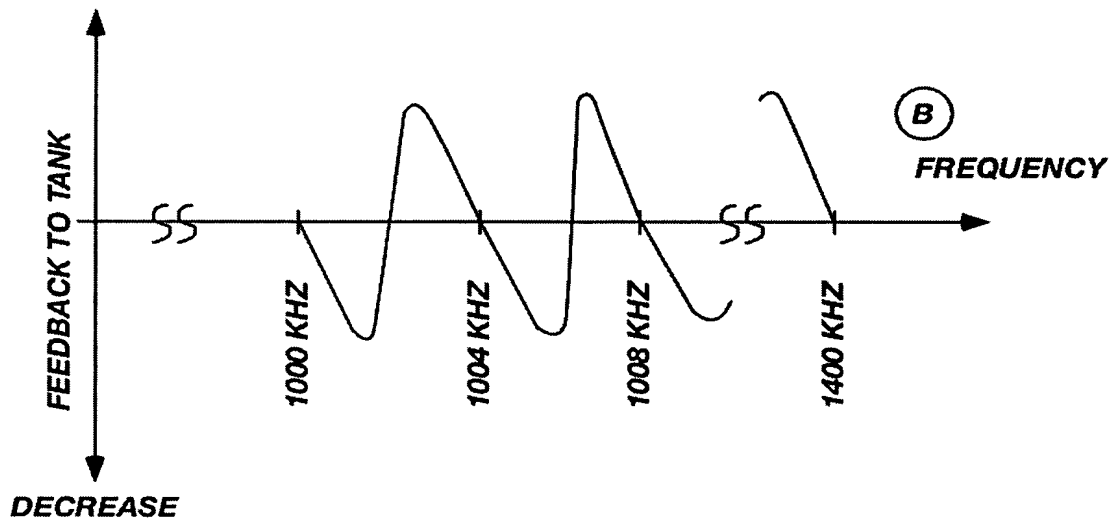


FIG. 8

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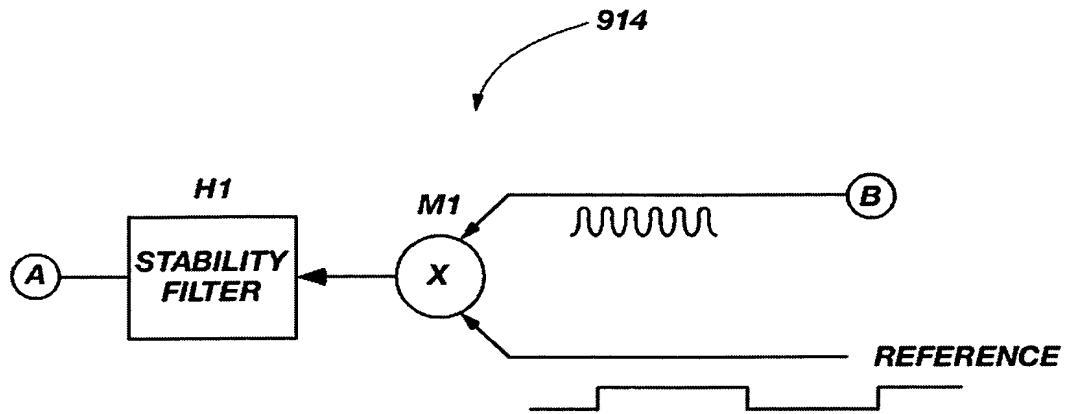


FIG. 9

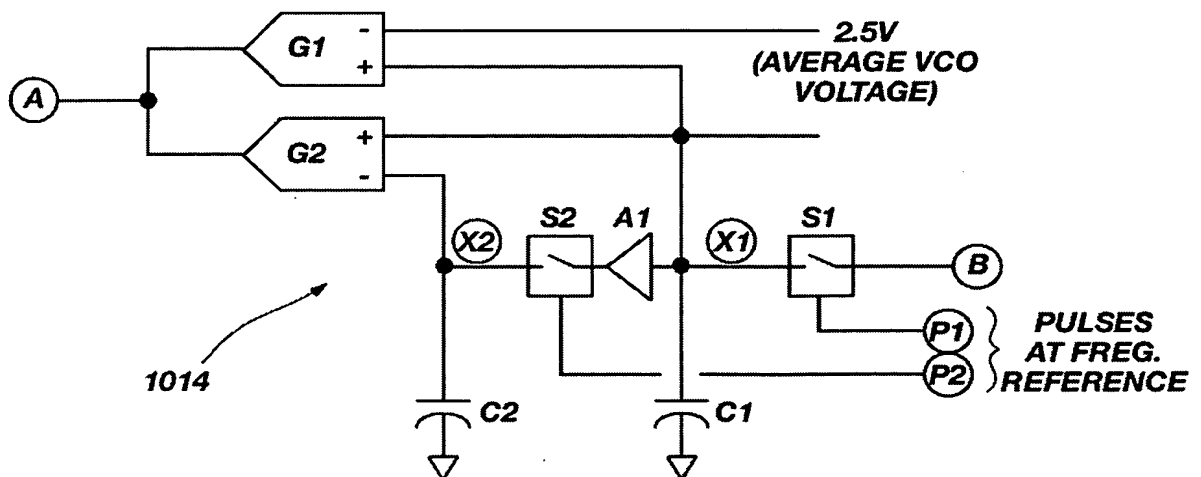


FIG. 10

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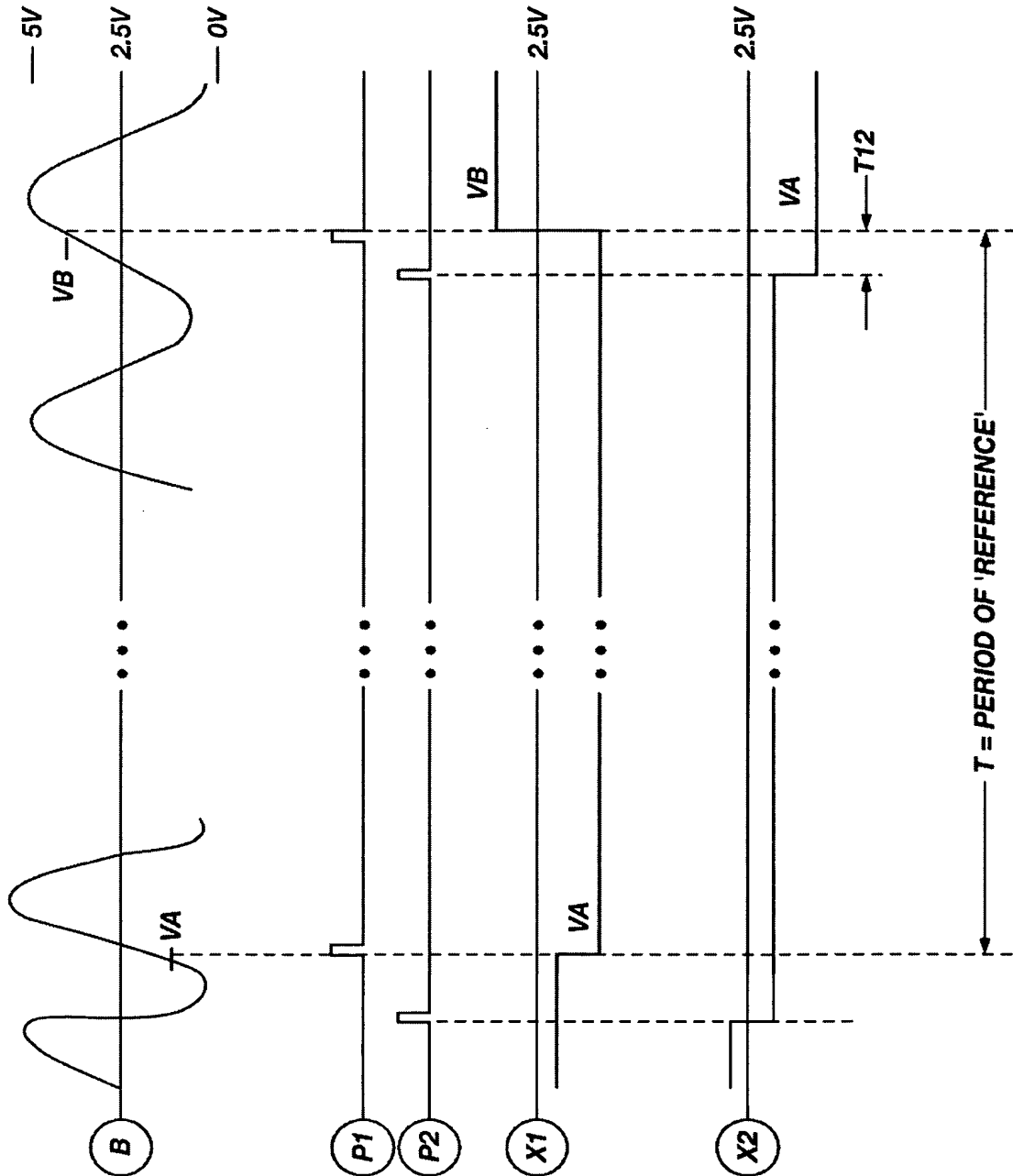


FIG. 11

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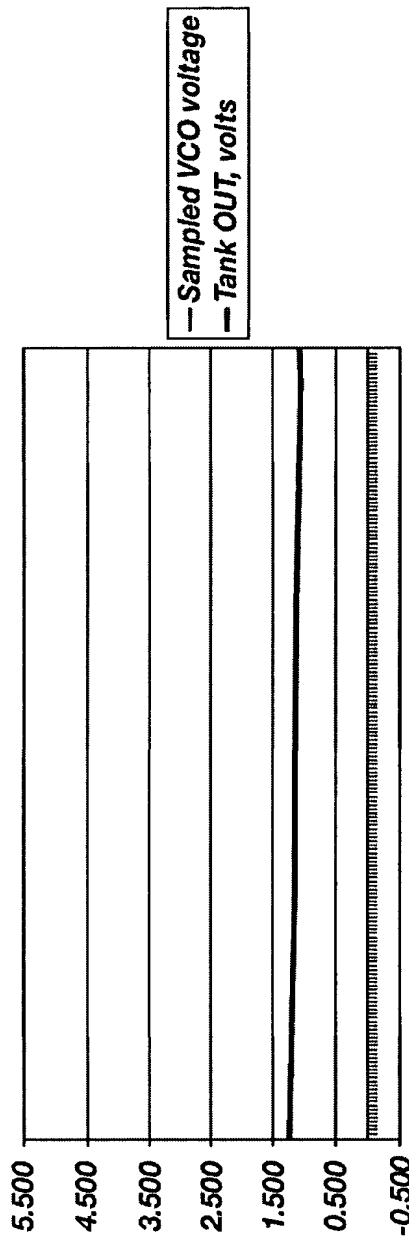


FIG. 12

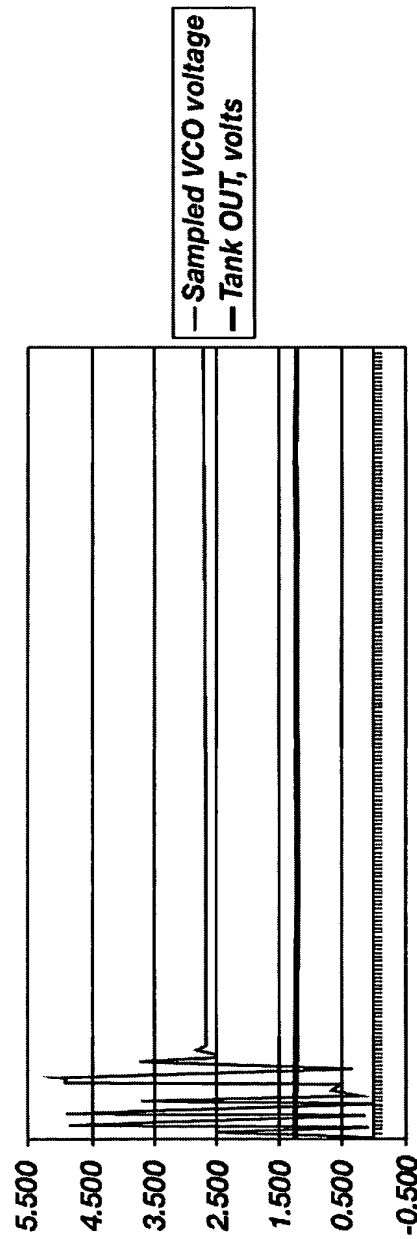


FIG. 13

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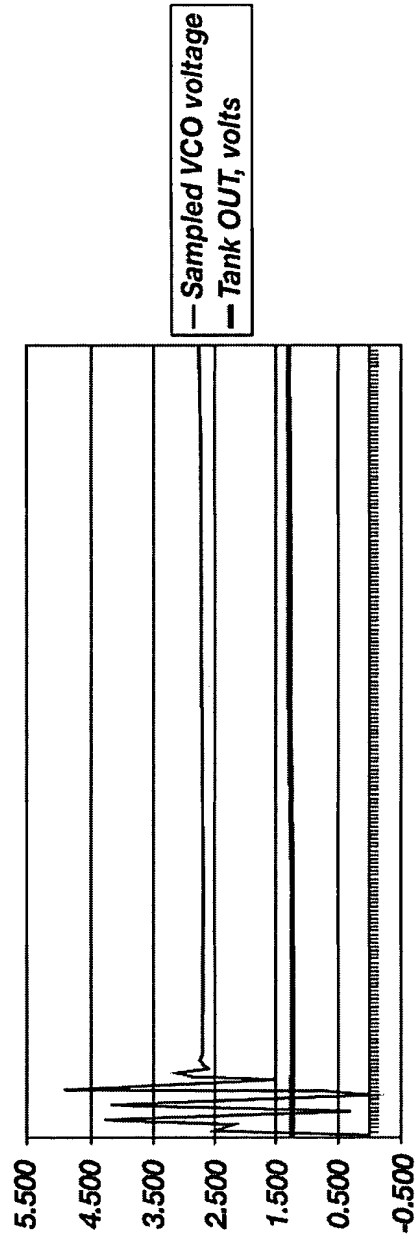


FIG. 14